METHOD OF MAKING A SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor memory device and to a method of fabricating the same. More particularly, it relates to a DRAM having memory cells, each including a capacitor and to a transistor and a method of fabricating the same.

2. Description of the Related Art

In a conventional method of fabricating a semiconductor memory device having memory cells, an element isolation insulating film is formed on the surface of a semiconductor substrate by LOCOS process and then the memory cells are formed. However, since bird's beaks develop during the formation of this element isolation insulating film, the prior art method involves a problem that a semiconductor memory device having memory cells integrated at a high density cannot be fabricated so easily.

To solve this problem, as disclosed, for example, in "Isolation Process Using Polysilicon Buffer Layer for Scaled MOS/VSLI", Yu-Pin Han and Ring Ma, The Electrochemical Society Extended Abstract, 1984 and JP-A-63-302536, an improved LOCOS process using a polysilicon buffer layer for the formation of the element isolation insulating film has been proposed to reduce the bird's beaks.

A method of fabricating a semiconductor memory device using a polysilicon buffer layer will be explained with reference to FIGS. **3A** and **3B**. First of all, an element isolation insulating film **102** is formed on the surface of a silicon substrate **101** by an improved LOCOS process using a polysilicon buffer layer as shown in FIG. **3A**, and capacitor trenches **103** are then formed by a reactive ion etching (RIE) process. Next, a first capacitor electrode film **104**, a capacitor insulating film **105**, a second capacitor electrode film **106**, a gate insulating film **107**, a gate electrode **108** and diffusion layers **109** to serve as drain and source regions of a transistor are successively formed.

According to this method using the polysilicon buffer layer, however, the step of forming the polysilicon layer is necessary. Therefore, the steps become more complicated, and a design margin is necessary in consideration of an alignment error of a mask at the exposure step of forming the element isolation insulating film and deviation in the process. For these reasons, there is a limit in reducing the width of the element isolation insulating film, and it is indeed difficult to satisfactorily integrate the memory cells at a high density.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor memory device including at least one memory cell having a transistor and a trench capacitor, wherein the memory cell is formed in a limited area on a semiconductor substrate.

Another object of the invention is to provide a method of fabricating a semiconductor memory device including at least one memory call having a transistor and a capacitor in which the memory cell is formed in a limited area on a semiconductor substrate.

To achieve the above object, according to the present invention, a semiconductor memory device, which includes at least one memory cell having a transistor and a trench capacitor, comprises a semiconductor substrate having a surface in which at least one trench is formed so as to define two areas on the surface of the semiconductor substrate separated by the trench; a transistor having source and drain regions formed on the surface of the semiconductor substrate at its first area disposed at one of two opposite sides of and adjacent to the trench; a polysilicon layer formed to be in contact with one of the source and drain regions and to extend over an inner surface of the trench and a second area of the surface of the semiconductor substrate disposed at the other side of the trench; and a silicon dioxide region formed by oxidizing a part of the polysilicon layer extending on the second area of the surface of the semiconductor substrate.

According to the present invention, a method of fabricating a semiconductor memory device, which includes at least one memory cell having a transistor and a capacitor, comprises the steps of: forming at least one trench in a surface of a semiconductor substrate; forming a semiconductor film so as to cover the surface of the semiconductor substrate and an inner wall of the trench; and processing the semiconductor film to form an element isolation insulating film and a conductor film serving as one of electrodes of the capacitor.

In the method of fabricating a semiconductor memory device including at least one memory cell having a transistor and a capacitor according to the present invention, since the element isolation insulating film is formed after the trench or trenches are formed, the width of the element isolation insulating film is limited and the occurrence of the bird's beaks is restricted by the trench so that the element isolation insulating film can be formed in a sufficiently small size with reduced bind's beaks. Further, the design margin for the alignment error of the mask at the exposure step of forming the element isolation insulating film and for process deviation, which has been necessary in the prior art method, can be reduced in the method of the present invention. Therefore, the memory cells can be easily integrated at a high density. Furthermore, since the element isolation insulating film and one of the electrode films of the trench capacitor can be formed of the same semiconductor film, the fabrication steps can be simplified.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** to **1G** are sectional views of a part of a semiconductor memory device at the respective steps in a method according to a first embodiment of the present invention;

FIGS. **2A** to **2D** are sectional views of a part of the semiconductor memory device at the respective steps, different from those of the first embodiment, in a method according to a second embodiment of the present invention; and

FIGS. **3A** and **3B** are sectional views of a semiconductor memory device at the respective steps in a prior art method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention will be described with reference to FIGS. **1A** to **1G**.

In this embodiment, capacitor trenches **2** are first formed in a silicon substrate **1** having one conductivity type by a reactive ion etching (RIE) process, for exam-